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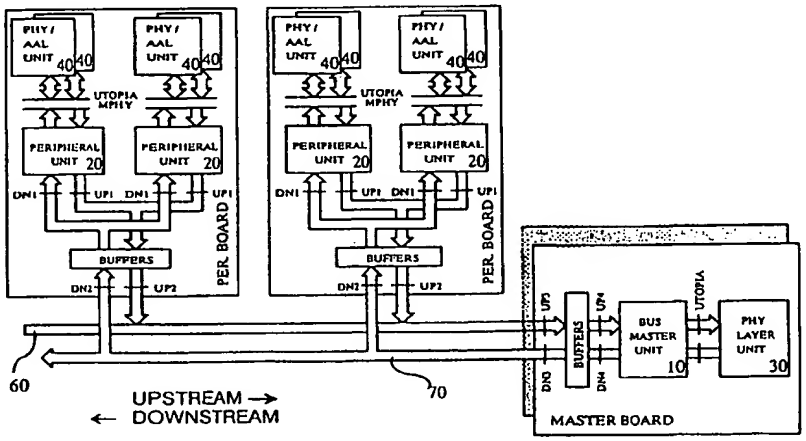

(57) Abstract

Multiple access communication system including: a central unit (10); a plurality of peripheral units (20-20), connected to the central unit through a connecting means to which fix-length data packets are transmitted from said central unit (10) to said peripheral units (20-20), and vice versa. According to the invention, said connection means includes: a first, dedicated, monodirectional data connection (70) (Cell_Start_DN, Data_Clk_DN, Data_DN), where the transmission of each data packet is made in a first fixed time period (T1); a second connection (60) including a monodirectional data connection (610) and a bi-directional control connection (620), where the transmission of any one of the data packets is made in a fixed second time period (T2). Thanks to the particular configuration of the above-mentioned connection means, it is possible to supply a flexible central control in the direction going from the peripheral units (20-20) to the central unit (10) in order to limit the cost of peripheral units. The invention enables to limit the processing complexity at central unit level (10).

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SYSTEM FOR DATA TRANSMISSION BETWEEN A CENTRAL UNIT AND A PLURALITY OF PERIPHERAL UNITS THROUGH A HIGH SPEED SYNCHRONOUS BUS

Field of the Invention

The present invention relates to broad band telecommunication systems and, more in particular, to a system for the transmission of data from more peripheral units to a central unit and vice versa.

The last years recorded an acceleration in the demand of high transmission speed by the users having access to the public telecommunication network. This was true up to now mainly for large business users having branches spread over the territory, and the suppliers of telecommunication services answered by furnishing dedicated or packet switching lines (such as, for instance, X.25, Frame Relay or SMDS). More recently, the exponential growth of Internet, the increased interest for the access to multimedia services through the telecommunication network, and the expected increase of telework (telecommuting), highlighted the need to enable also the small business users and even residential users to have access to the public telecommunication network with transmission speeds higher than the present ones. Among the emerging communication techniques, the ATM technique, acronym for Asynchronous Transfer Mode, deserves a particular interest due to its flexibility and effectiveness in supplying even very high bandwidths.

An evolution of the access network is foreseen for the next years both for the higher transmission speed used on said network and for the typology of the services that shall be offered through the same. Therefore, it shall be necessary to offer an access to the public telecommunication network at high speed, reliable, low-cost and suitable to receive different type of traffic coming from a plurality of different sources (or users), with traffic characteristics and service features even very different among them, in particular, but not only, for the requested transmission speed.

Therefore, in the last years a plurality of access networks to the public telecommunication network have been developed. One of these networks is described in the Italian patent application no. MI 96A 001064, under the name of the same applicant, where the above mentioned access network consists of a broad band, passive optical network or PON (Passive Optical Network) interconnecting a line termination (Optical Line Termination or, shortly OLT), generally located close to a

switching exchange, to a plurality of network units (Optical Network Unit or ONU in short), typically located close to the users.

The passive optical network forming the so-called network infrastructure, typically has a tree structure, that is point-multipoint, where the root is connected to the OLT and the terminal branches to each ONU, and consists of sections of optical fibre interconnected by passive optical components called power splitter/combiners, enabling to divide on the outputs or re-combine on a single output the signals reaching their inputs.

The system of the present invention, hereinafter defined ATM BUS has its preferred application field in the above mentioned access network to collect the communication traffic, preferably ATM, coming from multiple input interfaces and to send communication traffic, preferably ATM, towards the same, particularly when different transmission speeds (bit rate) are present. In particular, one of these preferred applications is inside the above mentioned Optical Network Units or ONU to convey the data coming from a plurality of peripheral units to the PON, through a BUS Master, unit, as better described below.

Other possible applications are for instance inside service or access multiplexers based on ATM technique.

Background art

WO 95/08887 discloses a source traffic control and asynchronous data transmission system including a master of the bus and a plurality of bus users coupled to a bi-directional data bus, said system, having a particular application in arranging the transfer of ATM cells in broad band ISDN systems.

The system employs a frame format of fifteen or sixteen cycles of system clock, which include a field for the request to bus access from the users and an access grant field. The arbitration algorithm for the access to the bus is implemented in the bus master unit and can be unknown to the bus users.

This system appears particularly useful to switch the traffic among the different units of the bus, irrespective of the fact that they are master or bus users. However, the system appears too complex for applications requiring to collect the traffic from a plurality of peripheral units (bus users) towards a single central unit (bus master) and to distribute the traffic from said single unit to one or more (possibly all) peripheral units.

In fact, in this case the presence of a bi-directional bus is not requested since the packets (cells) of data are not switched between the peripheral units. Moreover, in

some cases, it is useful that the transmission speed between the central unit and the peripheral units is different (generally higher) than the transmission speed in the opposite direction (that is, from peripheral units to central unit).

Finally, in this embodiment the central unit can know if a peripheral unit requires the access to the bus, but it seems not able to know the status of each single queue of each peripheral unit, so a limitation exists in the type of bus access management which can be controlled at central level.

In general, we can say that the above mentioned patent application does not make known in any way the methods for the implementation of a central control aimed at limiting the complexity of the peripheral units with consequent important cost reduction.

ATM Forum/95-0114R1 - Utopia Level 2 Specification, Version 0.8 - April 1995, discloses an interface between the physical layer and the ATM layer, called also UTOPIA M-PHY for the connection of a plurality of physical layer devices to a single ATM layer device. This interface is of particular interest for the flow control functions and relevant separation of the operation speed of the ATM layer versus those of the physical layer devices, enabling to have physical layer devices operating at different speed among them and different from the operation speed of the ATM layer device.

Said interface implies, from physical layer to ATM layer, a clock signal having direction opposite to the data transfer one (counter-directional) and, as it is specified, it appears it cannot be directly employed on a system where the peripheral interfaces are distributed on a plurality of peripheral boards connected to a backplane of significant size, said backplane connecting the peripheral boards to the single central interface, placed on a central board, mainly when the transmission between the central board and the peripheral boards occurs at high speed (e.g., up to 622 Mbit/s).

Also, this interface, as it is specified, does not appear effective to supply the central part (ATM layer) with a knowledge of the queue filling situation of a plurality of peripheral interfaces, as the number of said queues and/or interfaces increases.

Objects of the Invention

Object of the present invention is to identify a system for the exchange of data between a central unit and a plurality of peripheral units not showing the drawbacks and restrictions of the above mentioned solutions of the known type and in particular capable to collect and distribute in a cost-effective way the information of the communications of a plurality of users.

Summary of the invention

The previous problems are overcome and an advance is made in the technique through the system of the present invention, which is a high speed (up to 622 Mbit/s), synchronous bus (ATM BUS), performing an ATM based, structured bi-directional interface between a central part and a plurality of peripheral parts. It is based on two kinds of units, that is the Bus Master Unit (BMU = Bus Master Unit) and the Peripheral units (PU = Peripheral Unit), connected to the BMU through a shared connection means (bus). The BMU plays its role in the central part (master), while the PUs are associated to the peripheral parts (slave), and in particular they are placed on a peripheral board (PB = Peripheral Board) connected to the bus. Of course, more than one single PU can be installed on a single board, when allowed by the feasibility limits of the board itself.

A featuring characteristic of the present invention is the ability to furnish a central flexible control in the direction from the peripheral units to the central unit (upstream), that is from multi-point to point, as well as of course, in the opposite direction, that is from the central unit to the peripheral units (downstream). This enables to limit the cost of the peripheral units, maintaining reduced the processing complexity at central unit level, so to be cost-saving compared to point-to-point structures where the ATM functions (including the sector of traffic control) are dedicated to each input (peripheral) interface. Provisions can also be made for a redundancy mechanism of the central part, so to increase the system reliability.

An additional feature characterizing the present invention is the high flexibility in adding or replacing the PBs (or the PUs), which enables to update the system, saving the major part of the hardware already installed, since the greatest part of the functions are performed in the central part, this makes the ATM BUS an effective solution as for cost and therefore interesting to give access to the public network both to residential users and to the small/medium business users.

Furthermore, another advantage of the invention is the emulation of the UTOPIA M-PHY interface, which emerged as international standard for the connection of a plurality of physical layer devices to an ATM layer device.

Object of this invention is therefore a multiple access communication system, implemented according to what disclosed in claim 1.

The features of the present invention which are believed to be novel are set forth with particularity in the appended claims.

Brief description of the drawings

The invention, together with further objects and advantages thereof, may be

understood with reference to the following description, taken in conjunction with the accompanying drawings, and in which:

- Fig. 1 shows a functional block diagram of the ATM BUS according to the present invention:
- Fig. 2 shows the format of the data packet (cell) used by the ATM BUS;
- Fig. 3 shows the standard format of the ATM cell;
- Fig. 4 shows the diagram of the configuration of the bus upstream 60 of the ATM BUS of fig. 1;
- Fig. 5 shows the diagram of the configuration of the bus downstream 70 of the ATM BUS of fig. 1;
- Figs. 6 to 11 are time diagrams of the waveforms of the signals on the ATM BUS.
- Figure 12 shows a block diagram representing the BMU unit of figure 1.
- Figure 13 shows a block diagram representing one of the PU units of figure 1.

Detailed description of a preferred embodiment

The architecture of the ATM BUS (Fig. 1) is made of three main functional blocks: the Bus Master Unit (BMU = Bus Master Unit) 10, the Peripheral unit (PU = Peripheral Unit) 20, and the 60,70 connection means, respectively. The BMU 10 supplies an interface with physical layer device (PHY Layer) 30, this interface preferably being an 8-bit or 16-bit UTOPIA interface. Each PU 20 has an interface with physical level devices (PHY) 40 or ATM adaptation layer ATM (AAL = ATM Adaptation Layer) 40, said interface preferably being a UTOPIA Multi-Physical (M-PHY), 8-bit or 16-bit interface. The PUs transmit ATM cells to the BMU (upstream) and receive ATM cells from the same (downstream) through a high speed, synchronous, failure-enduring connection means (bus). In a preferred embodiment the bus is 16 bits of data and operated at 622 Mbit/s.

According to the invention, the 60,70 connection means consists of a UBUS (Upstream BUS) 60, transporting to the BMU data supplied at output by the PUs, and by a DBUS (Downstream BUS) 70 transporting to the Pus the data supplied at output by the BMU.

Each PU processes a plurality (e.g. 8) of peripheral ATM interfaces with PHY/AAL devices through the UTOPIA M-PHY. Each peripheral interface is associated to a single address of the UTOPIA M-PHY dedicated to the peripheral interface. Furthermore, the PU can process flows of diffusion channels (= broadcast VC) in the direction from BMU to PU (downstream), generating and addressing copies of the

cells to the corresponding PHY/AAL devices.

The BMU performs all the ATM layer functions, as the translation of the heading (= header translation) and the control of usage parameters (UPC = Usage Parameters Control), and acts as arbitrator for the accesses to the bus from PU to BMU (upstream) of the PUs through a specific interrogation protocol that shall be described below.

The ATM BUS consists, according to the invention, of two sections, separate from the logic point of view, one controlling the upstream flow and the other one the downstream flow. Both the sections have a gross throughput, for instance of (up to) 622 Mbit/s. The size of the ATM BUS cell is 54 bytes. For the preferred embodiment (16-bit data bus), in the downstream direction, 27 clock cycles are required to transport one 54-byte cell from the BMU to the PUs (on DBUS). In the upstream direction, 2 additional words (meaningless) are foreseen to supply an interruption in the transmission among cells, therefore 29 clock cycles are required to transport one 54-byte cell from a PU to the BMU (on the UBUS). This interruption is necessary to avoid that two PUs that transmit in succession, superimpose their transmissions on the bus due to the uncertainty in the phase in which each PU engages the bus, thus damaging the cells that would be received wrong for the last bytes of the preceding cell and the first bytes of the next cell.

The format of the cell transported on the connection means 60,70 (Fig. 2) shall be now described. In this description, the term cell is used to intend a predetermined group of bytes logically organized and transmitted as single entity, because the present invention is particularly oriented to ATM applications, which use the term cell to indicate a packet of 53 bytes. Other terms which can be used and intended included in the present invention, are frame or packet, so the following description could be considered valid also for the transmission of frames and/or packets.

The cell format on the connection means 60,70 is defined to enable a simple and effective transport of ATM cells from the BMU to the PUs and vice versa, considering the requirements of the cell format for the UTOPIA interface of Level 1. More in detail, the ATM header field (ATM header) and the UDF field (User Defined Field) can be transported in a transparent way through the bus in both directions, while an additional field (corresponding to the UDF2 field in the specific UTOPIA based on 16 bits of data) is configured to transport important proprietary information for the PUs and/or the BMU.

For the cell format at UNI (= User Network Interface), it shall be given the possibility to

transport in a transparent way the GFC field (= Generic Flow Control). In this case, in the upstream direction, the GFC field transparently crosses the PUs and the UBUS, and reaches the BMU, where the GFC can be terminated; in the downstream direction, the GFC in the cell coming from the BMU reaches the peripheral interface through the DBUS and the PU.

Where this function is not requested, in the upstream direction the GFC can be terminated at peripheral interface level (that is at the PU one), and no treatment of the GFC shall be made at BMU level, both for the upstream flow and the downstream one. If no transparent transport of the GFC is requested by the user at ONU level, in the position of the cell corresponding to the GFC field, an identification of the multiplexing group called Multiplex identifier (MID = Multiplex IDentifier) can be transported, which enables each physical layer interface (PHY) to multiples/demultiplex up to 8 ATM user flows per remote ATM interface. In this case, a Remote Termination Unit (RTU = Remote Termination Unit) (not shown), for instance placed at share level, will use the MID to multiplex/demultiplex the ATM flows of the relevant UNI interfaces.

The VPI, VCI, PTI and CLP fields of the standard ATM cell (Fig. 3) are processed by the ATM layer device, placed on the side of the BMU (or even integrated in the same). All the VCI, PTI and CLP fields, transparently cross the PUs, while the VPI field on the downstream flow can be modified as indicated below in case of broadcast/multicast flows.

The UDF field specified in the UTOPIA protocol, at 8 bits can be transparently transported through the ATM BUS between the UTOPIA interface of the PU and the UTOPIA interface of the BMU, and vice versa.

On the ATM BUS, in both the directions, ATM cells are accompanied by a Bundle Flow Identifier (BFI = Bundle Flow Identifier), grouping the whole ATM point-to-point flow relevant to a single peripheral ATM address or source interface. The PUs address the cells coming from their peripheral interfaces and from the UBUS according to the BFI and the corresponding address of the UTOPIA M-PHY. Advantageously, using the BFI, the PUs can control the cells without having to process the VPI/VCI information and therefore optimising the dimensions of the tables relevant to each active connection.

According to the cell format on the proposed connection means (see Fig. 2), the BFI has 6 bits and identifies up to 64 peripheral interfaces. To overcome this limit, it is foreseen the use of the four more significant bits of the first word (16 bit) of the cell as

an extension of the BFI (BFI_EXT), instead of MID, and also in this case the GFC cannot transparently cross the ATM BUS as said before. Using the BFI and the BFI_EXT 10 bits are available, therefore up to 1024 interfaces can be addressed on the PUs.

In the case of broadcast/multicast (point-multipoint) virtual channels (VC = Virtual Channel) the BFI is not valid and all the broadcast VC at ATM BUS layer are identified by a VPI value called VPI Broadcast (VPIb). The VPIb can be configured at any desired value. Each broadcast VC inside the VPI broadcast is identified by a VCI value. The PUs recognize the VPIb and use the VCI to address a local research table containing the broadcast/multicast routing information. The PUs translate the VPIb into a VPIb' value, which is a configurable VPI value, valid on the peripheral interface side, and generate copies of the cells without additional processing of the header. In the broadcast/multicast operation, the MID is not valid and the RTU is requested to perform additional broadcast/multicast functions.

In the case of point-to-point flows the VPI field transparently crosses the PUs, while in the case of broadcast/multicast flows, the VPI identifying the broadcast flows(VPIb) can be translated by the peripheral interface in a specified value (VPIb').

Going back to Fig. 2, provisions are also made for a HouSeKeeping field(HSK) to transport cell processing information (routing, copy, extraction) for the diagnostics of the bus and for operation and maintenance purposes. This field determines, both in the upstream and downstream directions, the type of treatment the cell will undergo. In the preferred embodiment the following coding for this field are given:

- 00: empty cell (that is, to be rejected at receipt since it does not transport significant data);
- 01: valid cell to send;
- 10: valid cell to extract toward microprocessor;
- 11: valid cell to be sent and copied for extraction towards the microprocessor.

We shall now describe the operation of the PU on the upstream flow. The PU receives the cells from PHY and/or AAL devices through the UTOPIA M-PHY protocol performing the multiplexing of the different physical layer flows in a unique ATM upstream flow, and makes the header of the 54-byte cell to be transmitted to the UBUS (see Fig. 2). The header is made writing in the four more significant bits of the first word the value of the GFC field (when this shall be allowed to pass in a transparent way) or the MID or the BFI_EXT value corresponding to the UTOPIA M-

PHY address of the source peripheral interface (which is associated to the BFI value described below). The PU knows the value to be applied on the basis of a written configuration, for instance in a record and valid at interface layer. The construction of the header continues writing the VPI, VCI, PTI, CLP fields and the UDF field of the 8-bit UTOPIA protocol, which are allowed to pass in a transparent way. The PU adds therefore the HSK value and the BFI value corresponding to the UTOPIA M-PHY address of the source peripheral interface. Then, the PU applies the header so obtained to the payload of the corresponding cell. The PU gives also a buffer storage to accept a burst of n cells from the UTOPIA interface. In the preferred embodiment, n is equal to 32. In this way, a single PU can process up to 32 RTU, provided that the PU can transmit on the UBUS at a bit rate equal to the sum of the transmission speeds of physical layer of the physical later interfaces (local or remote) connected to the same. As better described below, this implies that the PU will receive grants to transmit upstream according to the transmission speed so requested. The PU gives also the capability to insert cells in the upstream direction for diagnostic purposes, these being sent to the PU by the local microprocessor.

Once the PU has at least one cell available for the transmission, it sends a transmission request, according to what indicated below, and transmits a single cell on the UBUS only after receipt of the relevant grant. Therefore, the PU engages the UBUS for the time of transmission of one single cell coinciding with each grant received.

The operation of the PU on the downstream flow is as follows. The PU receives the cell from the ATM BUS and makes the header of the 53-byte cell. To do this, it identifies first if the cell belongs to a point-to-point or point-multipoint connection. In case of point-to-point flow, the PU directly routes the cell to the relevant queue on the basis of the BFI value (which identifies a specific peripheral interface). In the case of point-multipoint flow, identified by a particular VPI value (that is, VPIb), the PU employs the VCI value to address a local research table containing the routing information, that is the interfaces to which the copies of a cell belonging to the considered broadcast flow have to be sent; on the basis of this information the PU routes the copies of the cell to the relevant queues of the involved peripheral interfaces, without performing (in this case) a translation of the header, except for the translation of VPIb into VPIb'. Considering that the transmission speed of each single peripheral interface is lower (even significantly) than the transmission speed on the DBUS, a speed adjustment is requested in the PU made through a shared buffer

memory with separate queues for peripheral interface. On the downstream flow, the PU constructs the header of the 53-byte cell as follows. If the four more significant bits of the first word (16 bits) of the cell are occupied by the GFC or by the MID, they are written in the corresponding position of the output header. If, on the contrary, they are occupied by the BFI_EXT, this information is not written in the output header, but is locally controlled to associate the cell to the relevant output queue. Therefore, the PU copies the VPI, VCI, PTI, CLP and UDF fields (UDF1 of the 8-bit UTOPIA protocol) in the corresponding positions of the output header. Once the 53-byte cell is constructed, the PU sends it towards the PHY/AAL layer devices through the UTOPIA M-PHY interface. Flows are demultiplexed towards the relevant device and the PU associates the address peripheral interface to the corresponding UTOPIA M-PHY address. On the downstream flow, the PU offers the cell extraction possibility on the basis of the value of the HSK field, for instance for diagnostic purposes.

We shall now describe the operation of the BMU on the upstream flow. The BMU directs the timing of the upstream generating a clock of slot upstream (Slot_Stb_UP = Slot Strobe UPstream) defining the transmission time slots (time slot) for the PUs. Also, the BMU regulates the access to the bus upstream by the PUs. During each bus cycle, the BMU expects to receive the information of the availability of one cell (at least) (CLAV = CelL AVailable) from all the connected PUs and sends a grant to transmit (TxG = Transmit Grant) to a single PU. (The PU is selected on the basis of a specific algorithm implemented by the BMU, not described herein). The BMU obtains all the parameters for the ATM switching addressing a local research table; the address is supplied by the ATM layer identifiers (VPI, or VPI and VCI) and by the BFI (relevant to the source peripheral interface). The BMU translates the ATM headers of the cells entering the header. The UDF field (UDF1 of the 8-bit UTOPIA protocol) is copied in a transparent way. Therefore, the control functions of traffic parameters (UPC/NPC = Usage/Network Parameter Control) are made on the cells to decide whether to send or reject the same because not in compliance with what defined. Once the cells result complying with usage parameters, they can be stored in a buffer memory of speed adjustment to the physical layer interface, which can have lower speed. Finally, the BMU transmits the ATM cells to the physical layer device through the UTOPIA interface according to the requested transmission speed. On the upstream flow, the BMU performs also the following functions. It offers the capability of upstream cell extraction on the basis of the value of the HSK field to diagnosis purposes of the ATM BUS; enables the extraction of upstream cells on the basis of

the value of the BFI field and of the ATM header for OAM functions and extraction of channel services; it gives the possibility to insert upstream cells for OAM functions and service channels.

Following is the description of the BMU operation on the downstream flow. The BMU receives ATM cells from the physical layer device through the UTOPIA interface at the maximum speed (e.g. 622 Mbit/s). It provides a light buffer storage to conciliate the number of clock pulses requested to receive the cell of the incoming flow (27 clock pulses) with the number of clock pulses requested for the transmission of the cell on the DBUS (27 clock pulses plus 2 clock pulses for interruption on the bus). The BMU obtains the ATM switching parameters addressing a local research table with the specific fields of the ATM header, then it translates the ATM header of the cell entering the ATM header configured on the PU side, it adds the configured BFI value (relevant to the address peripheral interface) and adds the HSK configured value. The UDF field of the 8-bit UTOPIA protocol is copied in a transparent way in the corresponding position of the cell. The BMU therefore transmits the cell on the DBUS at the maximum transmission speed (e.g. 622 Mbit/s). The BMU gives the following cell extraction and insertion capabilities. The cells can be extracted from the downstream flow on the basis of the value of their ATM header for OAM functions and extraction of the service channels. The insertion capacity of downstream cells is provided to diagnostic purposes and for the insertion of service channels.

It is now described more in detail an arrangement for a preferred embodiment of the PMD layer, that is the merely physical layer through which signals are exchanged between the BMU and the PUs.

Figures 4 and 5 show the signals forming part of the ATM BUS: In particular, figure 4 shows the signals belonging to the part relevant to the upstream flow of the ATM BUS, or of UBUS 60. On the contrary, figure 5 shows the signals belonging to the DBUS 70.

In figure 4, it can be noticed that the signals of the UBUS 60 are organized as two separate buses: a monodirectional data bus 610 and a bi-directional control bus 620. The monodirectional data bus 610 is shared by the PUs 20-20 for the transmission of cells towards the BMU 10. The bi-directional control bus 620 is in its turn shared in a monodirectional control bus 621 to send control signals from the BMU 10 to the PUs 20-20, and in a shared monodirectional control bus 622 to send control signals from the PUs 20-20 to the BMU 10.

In figure 5, it can be noticed that the signals of the DBUS 70 are organized like a

monodirectional data bus for the transmission of cells from the BMU 10 to the PUs 20-20.

The meaning and use of the signals indicated in figures 4 and 5 will be more clear from the detailed description given now for a preferred embodiment of the PMD layer (= Physical Medium Dependent), that is the merely physical layer through which the signals are exchanged between the BMU and the PUs.

In a preferred embodiment the PMD is implemented through a parallel bus consisting of two separate sections for the upstream flow, UBUS, and downstream, DBUS. For both the sections the gross throughput is (up to) 622 Mbit/s with bus size of 16 bits and bus clock period of 26,5 ns (38,88 MHz frequency).

On both the bus directions the size of the ATM cell is 54 bytes. On the DBUS (that is, in the downstream direction), 27 clock periods have been used to transport a 54-byte cell from the BMU to the PUs. On the UBUS (that is in the upstream direction), 2 additional (empty) words are present, to supply an interruption in the transmission among consecutive cells, therefore 29 clock periods are used to transport a 54 byte cell (that is, 54 valid bytes and 4 empty bytes) from the PU to the BMU.

On the UBUS, all the PUs transmit cells being synchronized by the same bus clock, called slot upstream clock (Slot_Stb_Up), coming from the BMU, which acts as common reference. Each PU samples the slot clock using its 80 MHz clock to have an uncertainty of only half period of the 40 MHz clock (that is, 13 ns approx.).

The interruption mentioned above enables a maximum transmission skew (due to the dispersion of the characteristics of the technology employed) of 1 clock period (that is, 26,5 ns nominal for a 38,88 MHz clock) among the boards of the PUs on the backplane. Moreover, within a same board, one 1 clock period skew is allowed between two (or more) PUs.

The physical interfaces of the UBUS and DBUS are defined in the block diagram of Fig. 1.

In said block diagram, a general application is considered where on a single peripheral board more than one PU is located and auxiliary devices are used for the receipt and direction of uncoupling to guide the signals of the bus into high capacity/low impedance bus configurations.

The UP1, UP2, DN1, DN2 interfaces relate to the PU and interfaces DN3, UP3, DN4 and UP4 relate to the BMU.

The differences between interfaces UP1 and UP2 mainly consist of additional signals for the 3-state control of uncoupling pilot devices by the PUs. There is no real

difference between interfaces DN1 and DN2, except for the logic point of view. When more than one DN1 interface is present on the same board, the same can be placed in wired-OR configuration (wired-OR). The same applies to interfaces UP1.

The DN3 interface differs from the DN4 interface due to the fact that some timing and control signals can be divided into point-to-point configuration towards the other boards through uncoupling pilot devices to obtain the best quality of the signal at the receiver. The same considerations apply to UP3 and UP4 interfaces.

Following is the description of the signals of DN1, UP1, DN4 and UP4 interfaces.

The interface on the downstream flow, PU side, called DN1, consists of a clock Data_Clk_DN input, a 16-bit Data_DN input data bus, a Cell_Start_DN input signal and a 6-bit input bus (optional, though recommended) CRC6_DN. Data_Clk_DN is used to sample (on the ascent front) all the signals of the interface DN1; in a preferred embodiment, the frequency of Data_Clk_DN is 38,88 MHz. Data_DN is the bus on which the cell words (16 bits) are received, for a throughput of 622 Mbit/s. Cell_Start_DN is the signal which, when is at 0 (low active), marks the first word of the receipt cell (of 54 byte equivalent). CRC6_DN is the 6-bit bus on which the cyclic redundancy code word is received (CRC = Cyclic Redundancy Code) which protects the corresponding 16-bit word; this enables the receipt PU to detect single and multiple errors and to correct single errors.

The interface on the upstream flow, PU side, called UP1, consists of a clock input Slot_Stb_UP, an input TX_Gran_UP, an output clock Data_Clk_UP, a 16-bit output data bus Data_UP, an output signal Cell_Start_UP, a 6-bit output bus (optional through recommended) CRC6_UP, an output signal Data_TX_En_UP and a pair of output signals Clav0_UP and Clav1_UP. Slot_Stb_UP is the reference slot clock, supplied by the BMU to the PUs to mark the upstream cell transmission slots; the PU synchronize the transmission of the upstream cell with this signal. TX_Grant_UP is the signal indicating the grant to transmit, that is the signal enabling a specified PU to engage the upstream bus during the next upstream slot (indicated by Slot_Stb_UP) with the transmission of a complete cell. Data_Clk_UP is the reference clock of data transmission and is used by the Pus to generate (on the ascent front) the upstream transmission signals. Data_UP is the bus on which the words (16 bits) of the cell are transmitted, for a throughput of 622 Mbit/s. Cell_Start_UP is the signal which, when at 0 (active low), marks the first word of the transmission cell (58 bytes equivalent). CRC6_UP is the 6-bit bus on which the code redundancy cyclic word is transmitted (CRC = Cyclic Redundancy Code) which protects the corresponding 16-bit word; this

enables the BMU to detect single and multiple errors and to correct single errors. Data_Tx_En_UP is set at 0 (active low) by the PU during the transmission of the upstream cell; it can be used to check the high impedance condition of uncoupling pilot devices of the PU. (The signals Data_TX_En_UP of the PUs inside the same board must be placed in OR configuration). Clav0_UP or Clav1_UP is used by the PU to indicate to the BMU that it has (at least) one cell available for the transmission; each PU is configured to use Clav0_UP or Clav1_UP and to indicate the availability to transmit a cell, the PU sets at 0 the corresponding signal during 3 specified clock cycles. Clav0_En_UP or Clav1_EN_UP can be used to check the high impedance status of the uncoupling pilot devices during the transmission of Clav0_UP or Clav1_UP, respectively. The signals Clav0_UP or Clav1_UP of the PUs inside the same board must be placed in OR configuration.

The interface on the downstream flow, BMU side, called DN4, consists of an output clock Data_Clk_DN, of an output data bus Data_DN of 16 bit, of an output signal Cell_Start_DN, of an output bus (optional, through recommended) CRC6_DN of 6 bits and of a signal Data_TX_En_DN. All the signals of the interface are generated on the descent front of Data_Clk_DN; in a preferred embodiment, the frequency of Data_CLk_DN is 38,88 MHz. Data_DN is the bus on which are transmitted the words (16 bits) of the cell, for a throughput of 622 Mbit/s. Cell_Start_DN is the signal which, when at 0 (active low), marks the first word of the transmission cell (54 bytes equivalent). CRC6_DN is the 6-bit bus on which the cyclic redundancy code word is transmitted (CRC = Cyclic Redundancy Code) which protects the corresponding 16-bit word; this enables the receipt PU to detect single and multiple errors and to correct single errors. Data_TX_En_DN is slaved by the BMU during the transmission of the upstream cell and can be used to check the high impedance condition of the uncoupling pilot devices in the case of a configuration with multiple load-shared BMUs.

The interface on the upstream flow, BMU side, called UP4, consists of a slot clock output Slot_Stb_UP, a TX_Gran_UP output, an input clock Data_Clk_UP, a 16-bit input data bus Data_UP, an input signal Cell_Start_UP, a 6-bit input bus (optional, through recommended CRC6_UP, a pair of input signals Clav0_UP and Clav1_UP. Slot_Stb_UP is the reference slot clock, supplied by the BMU to the PUs to mark the transmission slots of upstream cell; the PUs synchronize the transmission of he upstream cell with this signal. TX_Grant_UP is the signal indicating the grant to transmit, that is the signal enabling a specific PU to engage the upstream bus during

the subsequent upstream slot (identified Slot_Stb_UP) with the transmission of a complete cell. It is organized as a 10-bit sequence in which the first bit is the validation of the sequence (when set at 0, active low); the next 8 bits code the identified of the PU and the last bit is an odd parity bit for the 10-bit sequence. The first bit of TX_Grant_UP is sent coinciding with the signal Slot_Stb_UP. Data_Clk_UP is the reference clock for data transmission and is used by the BMU to sample the upstream transmission signals (in the descent front). Data_UP is the bus on which the (16-bit) words are received for a 622 Mbit/s throughput. Cell_Start_UP is the signal which, when at 0 (active low), marks the first word of the receipt cell (58 bytes equivalent); the BMU employs it to align to data received. CRC6_UP is the 6-bit bus on which the cyclic redundancy code word is received (CRC = Cyclic Redundancy Code) protecting the corresponding 16 bit word; this enabled the BMU to detect single and multiple errors and to correct single errors.

Clav0_UP and Clav1_UP are used to indicate to the BMU that one cell (at least) is available for the transmission by one (ore more) PUs.

The nominal timing relations are shows in Figures 6 through 11, for DN1, UP1, DN3 and UP3 interfaces. It is considered immediate to obtain the corresponding relations for interfaces DN2, UP2, DN4 and UP4 (Fig. 1). Making reference to the timing diagrams of interface UP3 (Figures 10 and 11), it is worth to notice that the upstream signals of the backplane include eight wires for Data_Clk_UP, thus enabling to limit (up to) eight PU boards at the BMU board (and therefore to a maximum of 16 PUs, in case of 2 PUs per board).

We shall now describe the behavior of the BMU 10 and of PU 20-20 making reference to the relevant diagrams shown in Figures 12 and 13.

On the downstream flow, the BMU 10 receives the cell from the input port 101, it processes the header in block 102 translating the same into the proprietary format, and sends it to the PUs 20-20 through the monodirectional data bus 70 through the block 103. Each PU 20-20 receives the cell through the block 201, in block 202 it checks if the cell is destined to the same and if there is a cell requesting to be sent to more than one output of the PU 20 (multicast), in this case placing the cell in each one of the queues specified inside the block 203; the cell is thus translated again into the ATM standard format by the block 204 and is sent at output to the UTOPIA M-PHY interface through the block 205. The block 203 temporarily stores the cells, organizing the same in a plurality of queues, a queue for each one of the physical layer units/AAL 40-40, so to make a speed adjustment between the speed on the DBUS 70

and the speed (lower) at the UTOPIA M-PHY interface.

On the upstream flow, the PU 20 receives the cell from the input port 206, it processes the header in block 207 translating the same into the proprietary format and temporarily stores it in the buffer memory 208. In this buffer memory, the cells are stored according to different queues, each queue being associated to one of the physical layer units/AAL 40-40. In a preferred embodiment, each physical layer unit/AAL 40-40 can have more than one queue associated, for instance two queues, having different service priority, for instance high and low. The control block 209 informs the block 211 of the availability of one or more cells in the buffer memory 208. The block 211 sends this information to the BMU 10 through the monodirectional control bus 622 piloting the signal Clav_UP (1:0) during the time slot specified for the PU 20, according to what described above.

The information of cell availability, supplied through the bus 622 at each cell time by all the PU 20-20 having to transmit one cell at least, are received by the block 110 of the BMU 10 and sent to the block 107 which controls the service order of the different queues of the PU 20-20.

The block 107 includes also means to store the type and status of one or more queues of each one of said peripheral units (20-20), and determine from which queue the data packet must be transmitted for a determined peripheral unit (20-20) which could occupy said shared monodirectional data connection, on the basis of the type and status of each one of said queues.

At each cell time, the block 107 identifies therefore from which queue a cell shall be extracted, it codes this information and sends it to the block 110 which sends it to the PU 20-20 through the control bus 621 adequately driving the signal TX_Grant_UP.

Each one of the PU 20-20 receives said signal through the block 211, decodes the same and sends it to the block 209, where it is checked if it identifies one of the queues from the PU 20 concerned. If this is true, the block 209 of the PU 20 directs the buffer memory 208 to read the cell in the specified queue and send it to the block 210 for the transmission on the shared monodirectional data bus 610 towards the BMU, according to the protocol described above for the data bus of the UBUS 60.

The cell is then received by the BMU 10 through the block 104, the compliance with traffic parameters is checked in block 105 (according to a 'leaky bucket' mechanism), and the block 106 processes the relevant header translating it again into the ATM standard format. Therefore, the cell is stored in the buffer memory 108 to adjust the transmission speed to the UTOPIA interface speed toward the physical layer unit 30

to which the cell is transmitted through the block 109.

Through the signals Clav0/1_UP and Tx_Grant_UP it is possible to realize control mechanisms with service priority at BMU central layer. In particular, a single PU can "own" more than one slot of the signal Clav0/1_UP, so to make separate requests, for instance, for queues requiring different service priorities. This can be useful to grant, for instance, a priority access to the bus to the cells of connections having real time service characteristics (real-time) versus the cells of connections without said characteristics. An example of a connection with real-time service characteristics is a connection transporting cells containing data originated by a video coder, while an example of connection not having said real-time characteristics is one transporting cells containing data for exchange of information between calculators (file-transfer). Finally, of course, if it were required to control at central level on cell basis a higher number of queues allocated in the PUs, it should be sufficient to add one or more other signals as Clav2_UP, Clav3_UP, etc., besides adding one or more bits to the Tx_Grant_UP signal, until the maximum number of queues requested can be accommodated.

The fact that the ATM BUS is a synchronous one, divided into fixed length slots, enables also an easy transport of the cells containing data relevant to samples originated in a synchronous ways, for instance voice PCM samples which must be transported in a synchronous way through the telecommunication network, in particular belonging to the so-called narrow band connections (Narrow-Band), meaning by this term the connections requiring transmission speed up to 2 Mbit/s.

From the above, it can be noticed that the BMU is able also to manage even sophisticated service disciplines (not dealt with herein) since it can avail of the situation of the queues of each single PU, on cell time basis. Moreover, the signals exchanged on the connection means (UBUS/DBUS) are similar to those exchanged at UTOPIA M-PHY interface level and therefore components available on the marked could be used and/or standard functions to implement the ATM and physical layer functions. Additionally, the limit due to counter-directional clock is overcome, being able to implement equipment including backplanes even of significant size.

Though the detailed description dealt with a preferred embodiment based on a bus including a plurality of data lines shared among the PUs, it should be clear to those who are skilled in the art that the objects of the present invention include the possibility to allow a certain independence from the merely physical part through which the signals are exchanged between BMU and PU. Therefore, a preferred

embodiment employing point-to-point connections between the BMU and the PUs to implement the shared means on which the signals are exchanged, preferably in serial mode, instead of on bus, has in any case to be considered as included in the ambit of the invention, since the sharing of signals is still present, and wanted, at the higher level, that is at the level of logic flows controlled by the BMU and by the PUs.

Therefore, while a particular embodiment of the present invention has been shown and described, it should be understood that the present invention is not limited thereto since other embodiments may be made by those skilled in the art without departing from the scope thereof. It is thus contemplated that the present invention encompasses any and all such embodiments covered by the following claims.

CLAIMS

1. Multiple access communication system including a central unit (10), a plurality of peripheral units (20-20), a connection means (70) adapted to connect said central unit (10) to each one of said peripheral units (20-20), and adapted also to transmit packets of data of fixed length from said central unit (10) towards said peripheral units (20-20),

and vice versa,

said central unit (10) including:

- means to receive information of cell availability (Clav0/1_UP), during an actual time period equal to a second, fixed time period (T2), coming from each one of said peripheral units (20-20) having at least one data packet available;
- means to determine, on the basis of said cell availability information (Clav0/1_UP), which peripheral unit (20-20) could occupy said shared connection means (60) for a time slot having duration equal to said second fix time period (T2) immediately next to the present time slot;
- means to transmit a grant signal (Tx_Grant_UP) identifying one among said peripheral units (20-20) identified by said means to determine,

and each one of said peripheral units (20-20) including

- means to transmit, in a time slot having duration equal to a third, pre-set fixed time period (T3), said cell availability information (Clav0/1_UP) concerning one of its queues;
- means to receive said grant signal (Tx_Grant_UP) identifying one among said peripheral units (20-20);
- means to transmit a packet of data following the receipt of said grant signal (Tx_Grant_UP) indicating that the peripheral unit (20-20) specified can occupy said second connection means;

said system being characterized in that:

a) said connection means (70) includes:

- a first dedicated monodirectional data connection (70) (Cell_Start_DN, Data_Clk_DN, Data_DN), where the transmission of each one of said data packages is made in a first fixed time period (T1);
- a second connection (60) including a monodirectional data connection (610) and a bi-directional control connection (620), where the transmission of anyone of said data packets is made in a second fixed time period (T2);

b) each one of said peripheral units (20-20) being adapted to communicate said cell availability information (Clav0/1_UP), for a specific queue or for more queues, by means of said bi-directional control connection during a time slot having duration equal to said third fixed time period (T3);

c) said central unit (10) being adapted to transmit said grant signal (Tx_Grant_UP) to all said peripheral units (20-20) through said connection of bi-directional control (620).

2. System according to claim 1, characterized in that:

said connection of bi-directional control includes a dedicated monodirectional control connection (621) and a shared monodirectional control connection (622);

each one of said peripheral units (20-20) communicates said cell availability information (Clav0/1_UP) for a specified or more of its queues on said shared monodirectional control connection (622) during a time slot having duration equal to said third fixed time period (T3);

said central unit (10) transmits said grant signal (Tx_Grant_UP) to all said peripheral units (20-20) through said dedicated monodirectional control connection (621).

3. System according to claim 1, characterized in that said means to determine (107) include means to store the type and status of one or more queues of each one of said peripheral units (20-20), and determine from which queue the data packet shall be transmitted for the determined peripheral unit (20-20) which could occupy said shared monodirectional data connection, on the basis of the type and status of each one said of said queues.

4. System according to claim 1, characterized in that said grant signal (Tx_Grant_UP) identifies a particular queue of one among said peripheral units (20-20), said queue being the one from which a data packet has to be transmitted during the time slot having duration equal to said second fixed time period (T2) immediately next to the present time slot.

5. System according to claim 1, characterized in that said time slot having duration equal to said third fixed time period (T3) has a pre-set position, different from that used by the other peripheral units (20-20).

6. System according to claim 1, characterized in that said means (107) to transmit a grant signal (Tx_Grant_UP) include means to code said grant signal (Tx_Grant_UP) before its transmission.

7. System according to claims 1 and 5, characterized in that said means (211) to receive said grant signal (Tx_Grant_UP) include means adapted to decode said grant

signal (Tx_Grant_UP) after its receipt, and means to detect which one of its queues, if any, is identified by the decoded value of said grant signal (Tx_Grant_UP).

8. System according to claim 1, characterized in that said means to transmit (210) a data packet include means to read (209, 208) said data packet from the particular queue identified by said decoded value.

9. System according to claim 1, characterized in that:

- said dedicated monodirectional connection (70) connects the data output of said central unit (10) at the data input of each one of said peripheral units (20-20);
- said shared monodirectional connection (610) connects the data output of each one of said peripheral units (20-20) at the input of data of said central unit (10);
- said dedicated monodirectional connection (621) connects the control output of said central unit (10) to the control input of each one of said peripheral units (20-20); and
- said shared monodirectional connection (622) connects the control output of each one of said peripheral units (20-20) at the control input of said central unit (10).

10. System according to claim 1, characterized in that:

- said shared and dedicated monodirectional data connections (610, 70) have a bus topology and consist of a first and a second plurality of wires respectively; and
- said shared and dedicated monodirectional control connections (622, 621) have a bus topology and consists respectively of a third and a fourth plurality of wires.

11. System according to claim 1, characterized in that said data and monodirectional control connections have a star topology, and said arbitration control unit (10) is placed at the star center.

12. System according to claim 1, characterized in that said data and monodirectional control connections have a tree topology, and said arbitration control unit (10) is placed at the tree root.

13. System according to claim 1, characterized in that said data packet has a fixed length of 27 words of 16 bits each.

14. System according to claim 1, characterized in that said data packet has a fixed length of 54 words of 8 bits each.

15. System according to claim 1, characterized in that said data packet transports the VPI, VCI, PTI and CLP fields of the header of an ATM cell and 48 byte of 8 bit of the payload of an ATM cell.

16. System according to claim 1, characterized in that said data packet transports 48 byte of 8 bits including one or more voice data samples, transmitted in a

synchronous way.

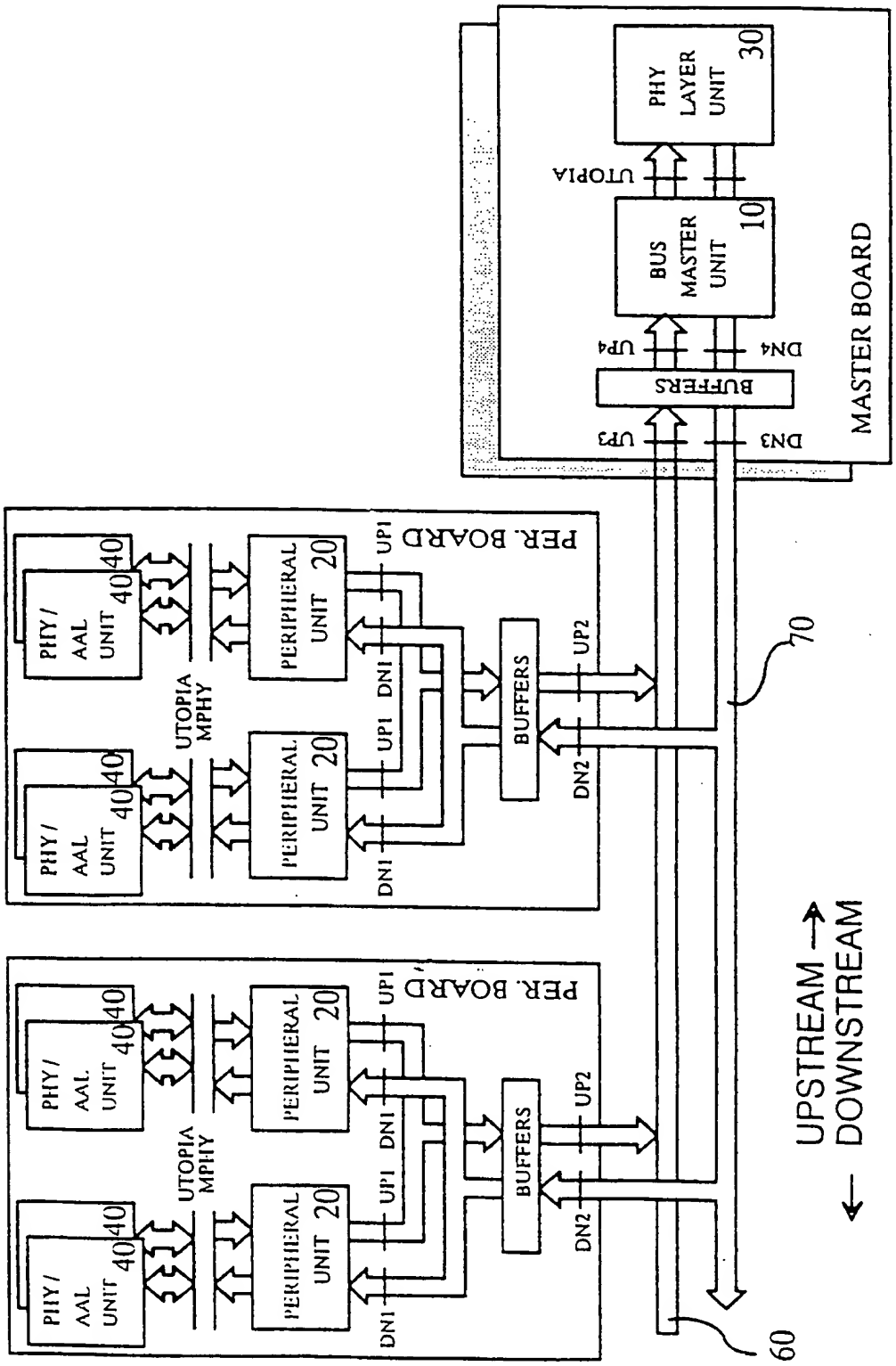


Fig. 1

GFC/MID BFI_EXT	VPI	VCI	
VCI		PTI	CLP
UDF/BFI_EXT	HSK	BFI	
P1	P2		
P3	P4		
P5	P6		
P7	P8		
P9	P10		
P11	P12		
P13	P14		
P15	P16		
P17	P18		
P19	P20		
P21	P22		
P23	P24		
P25	P26		
P27	P28		
P29	P30		
P31	P32		
P33	P34		
P35	P36		
P37	P38		
P39	P40		
P41	P42		
P43	P44		
P45	P46		
P47	P48		

Fig. 2

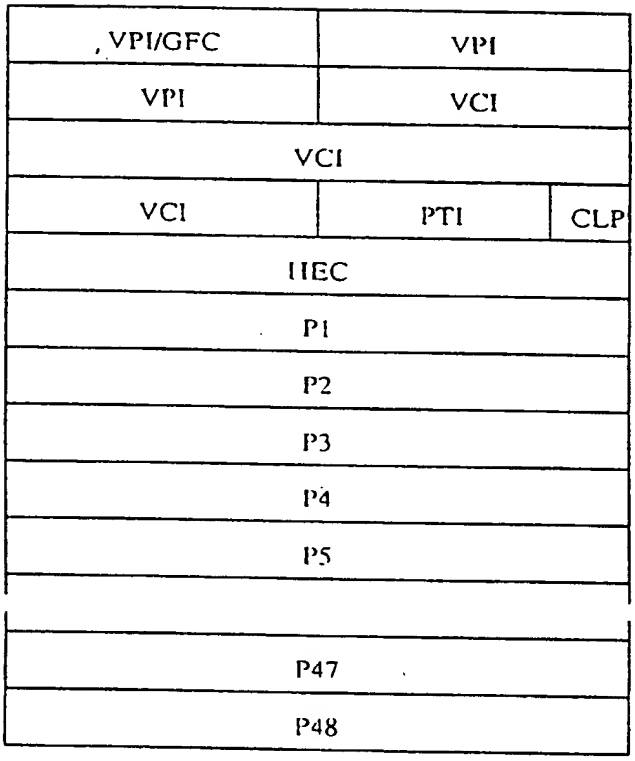


Fig. 3

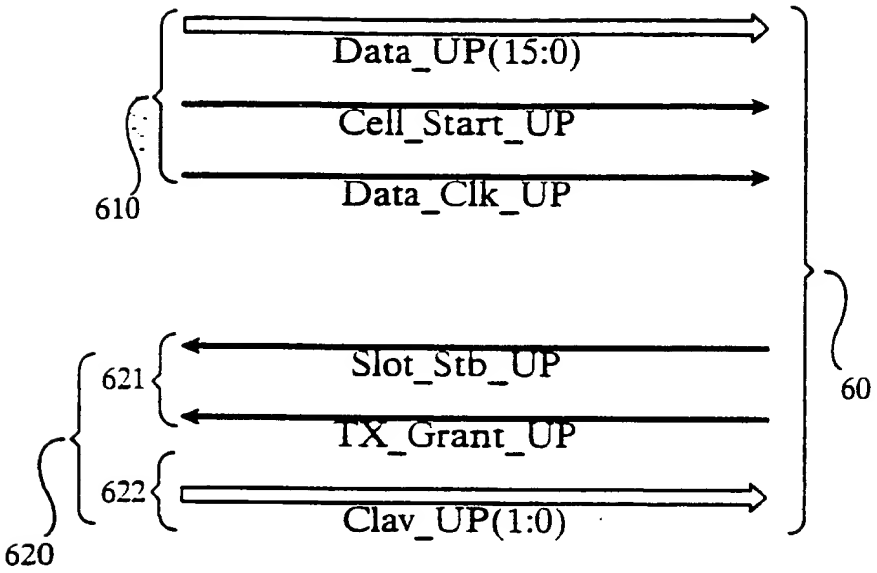


Fig. 4

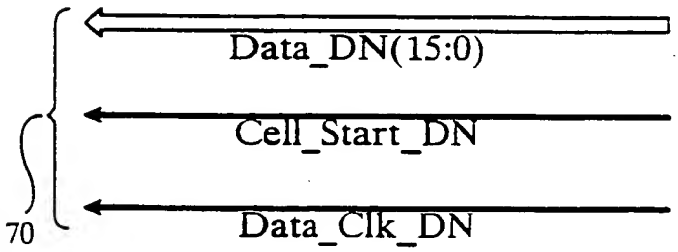


Fig. 5

Fig. 6

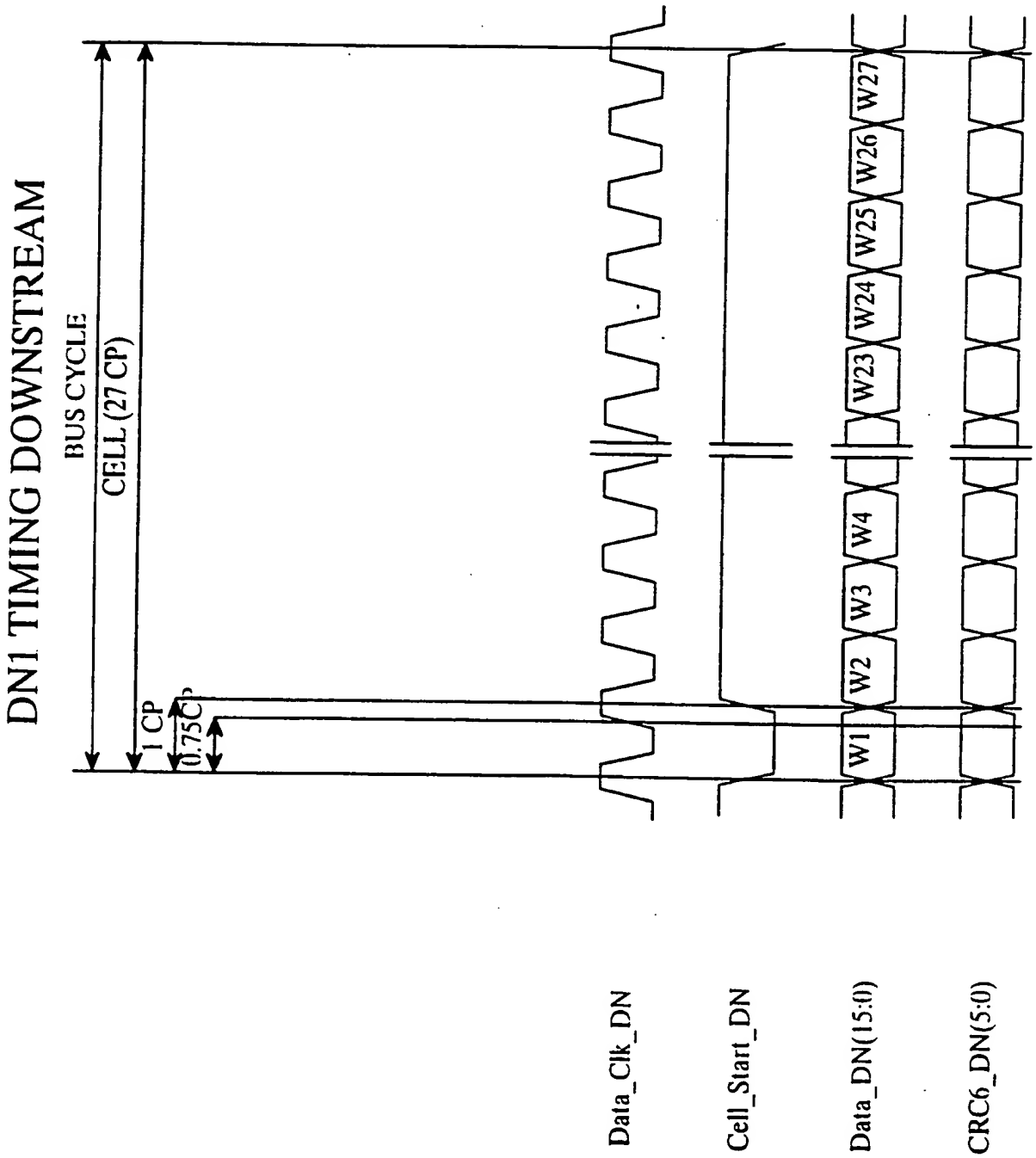


Fig. 7

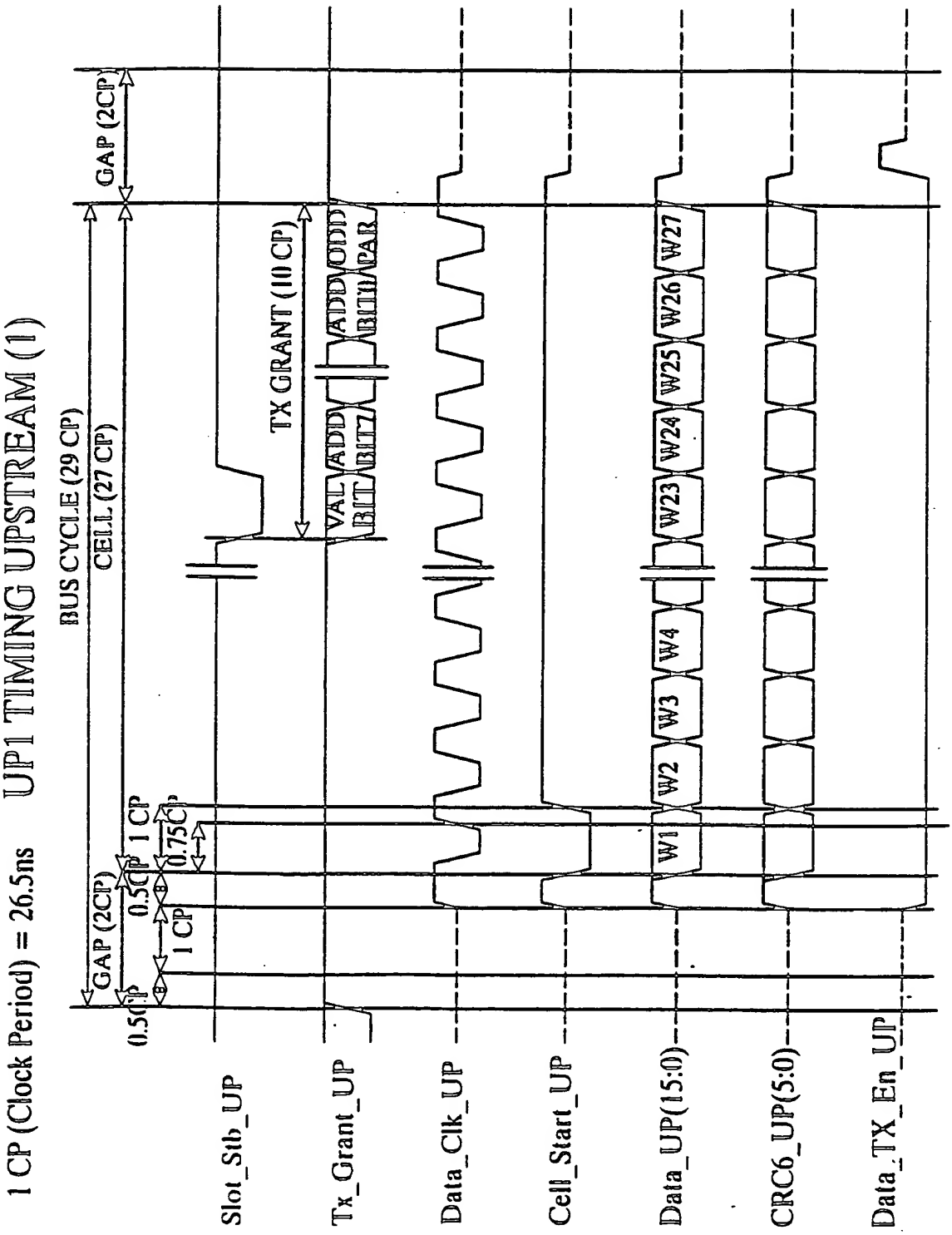


Fig. 8

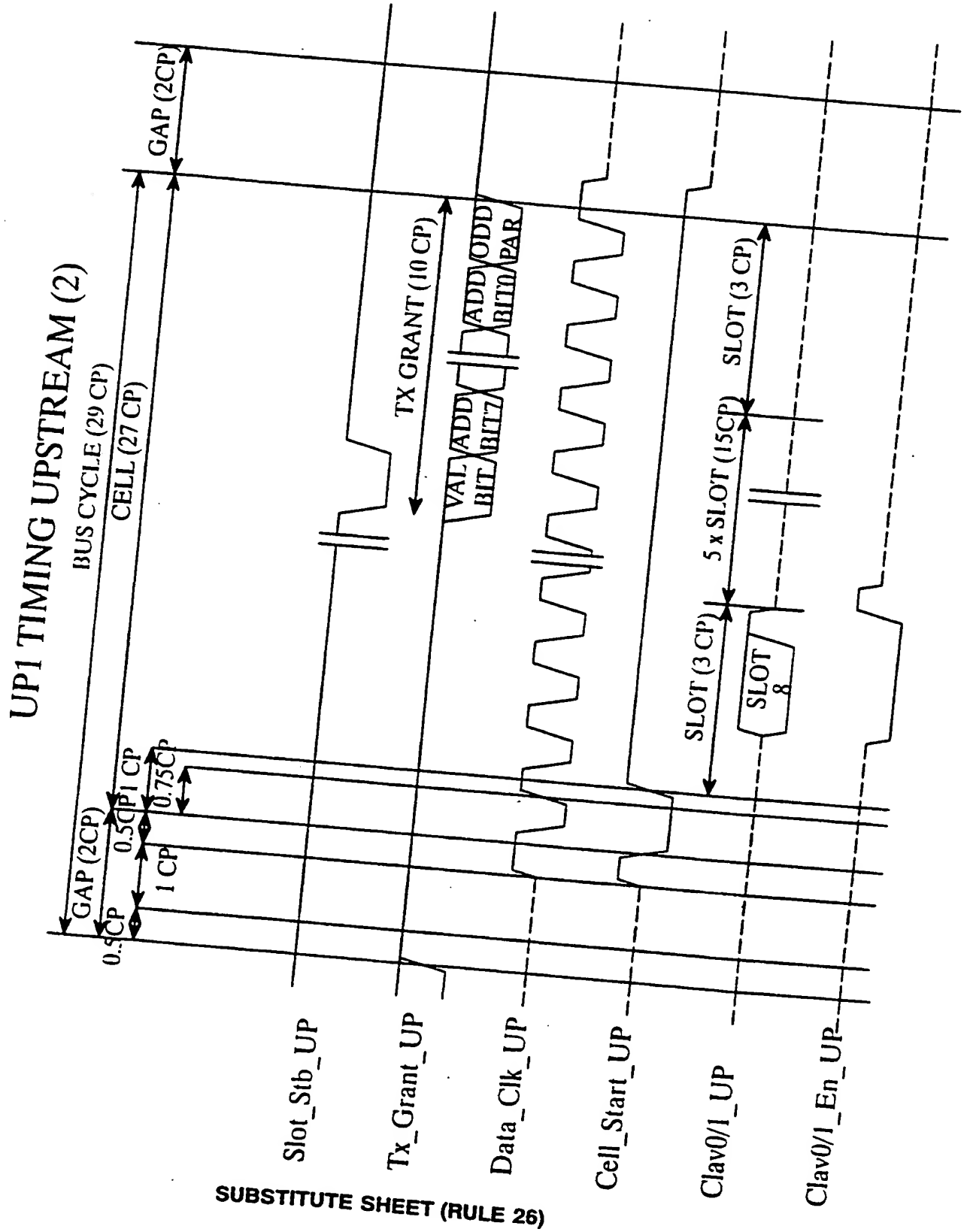

UP1 TIMING UPSTREAM (2)
BUS CYCLE (29 CP)
CELL (27 CP)
GAP (2CP)
TX GRANT (10 CP)
VAL
ADD BIT7
ADD BIT0
ODD PAR
SLOT (3 CP)
5 x SLOT (15CP)
SLOT (3 CP)
SLOT 8
GAP (2CP)
0.5CP
1 CP
0.75CP
1 CP
0.5CP
Slot_Stb_UP
Tx_Grant_UP
Data_Clk_UP
Cell_Start_UP
Clav0/1_UP
Clav0/1_En_UP

Fig. 9

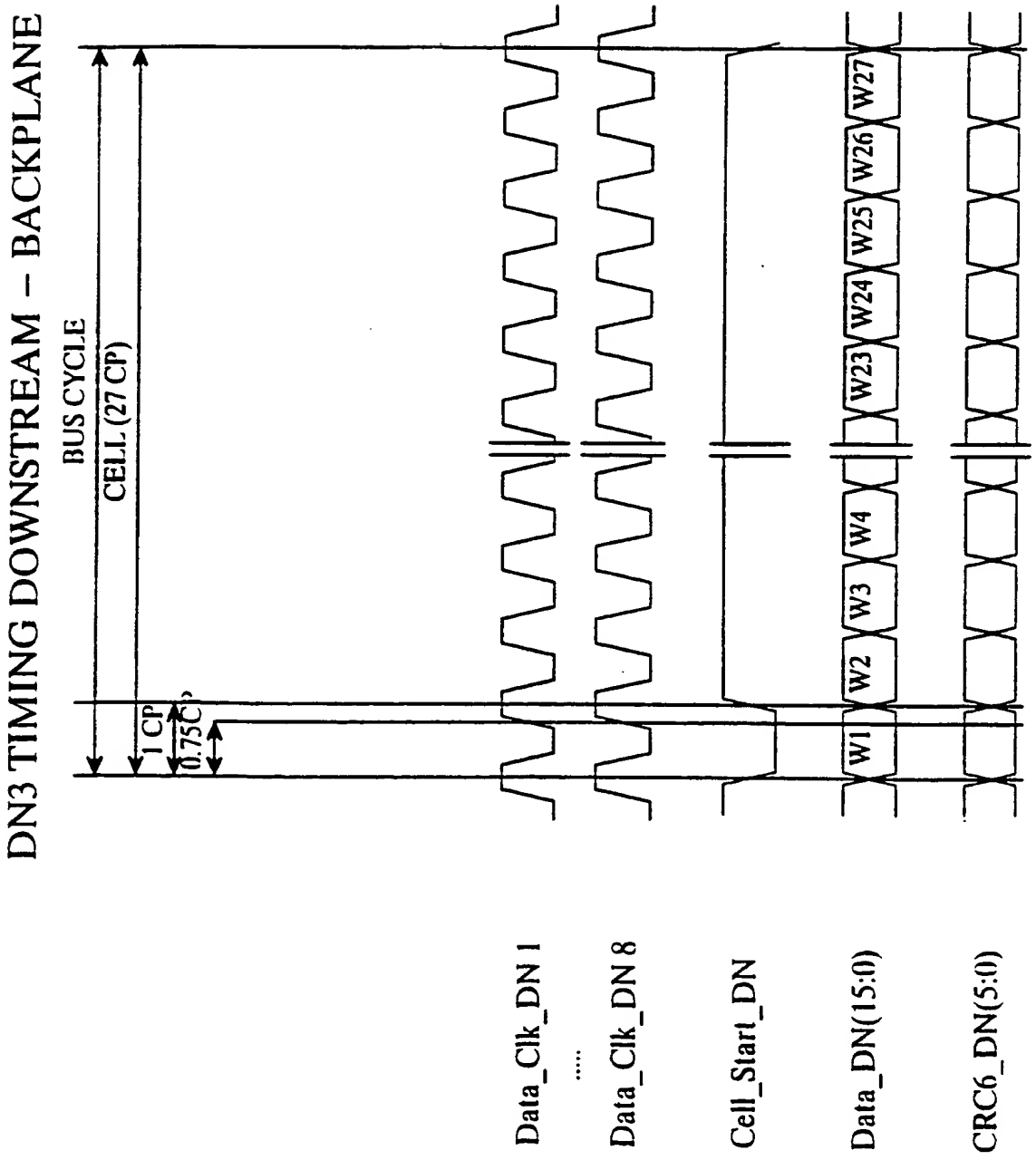

DN3 TIMING DOWNSTREAM – BACKPLANE
BUS CYCLE
CELL (27 CP)
1 CP
0.75CP
Data_Clk_DN 1
Data_Clk_DN 8
Cell_Start_DN
Data_DN(15:0)
CRC6_DN(5:0)
W1
W2
W3
W4
W23
W24
W25
W26
W27

Fig. 10

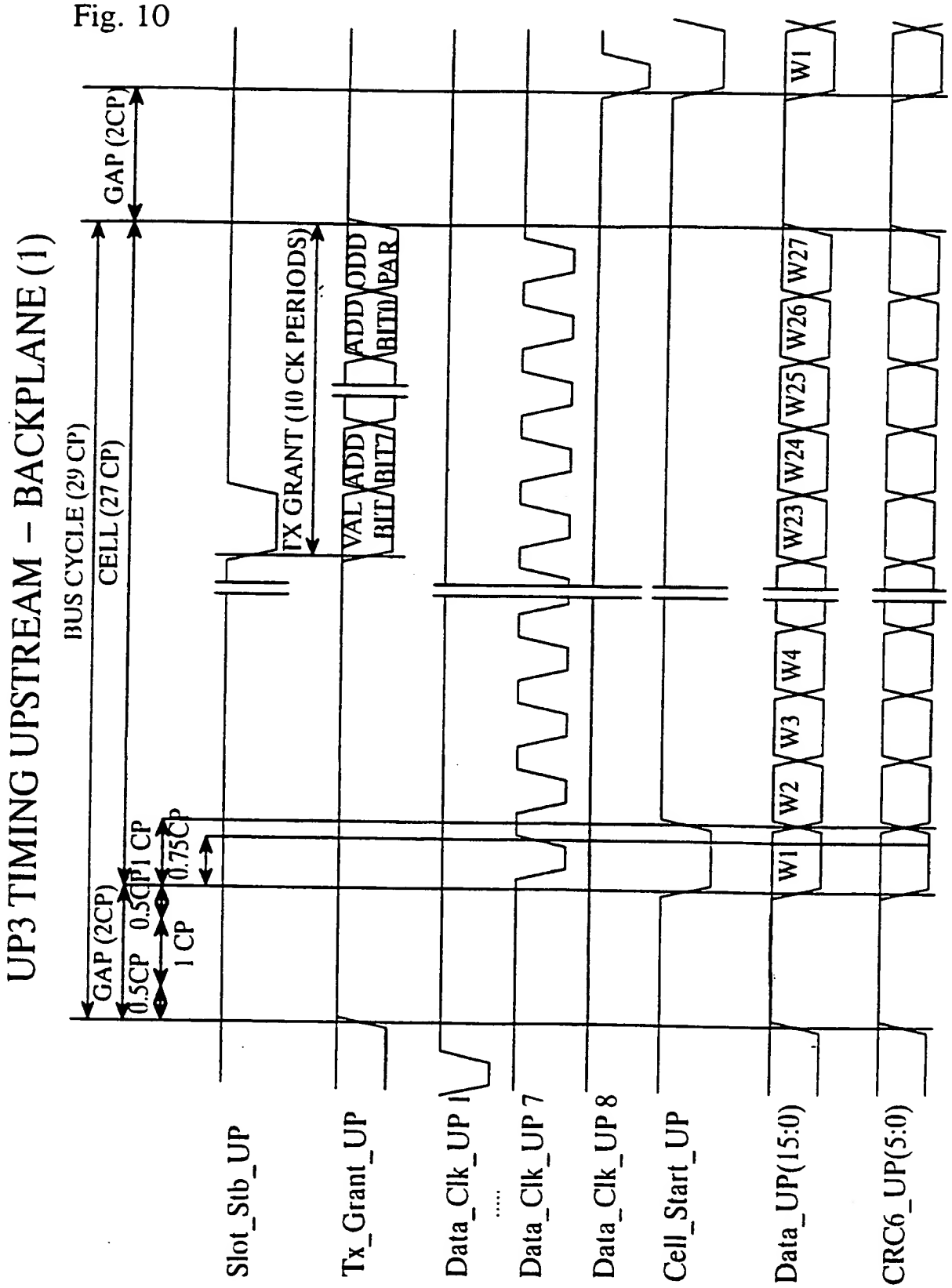
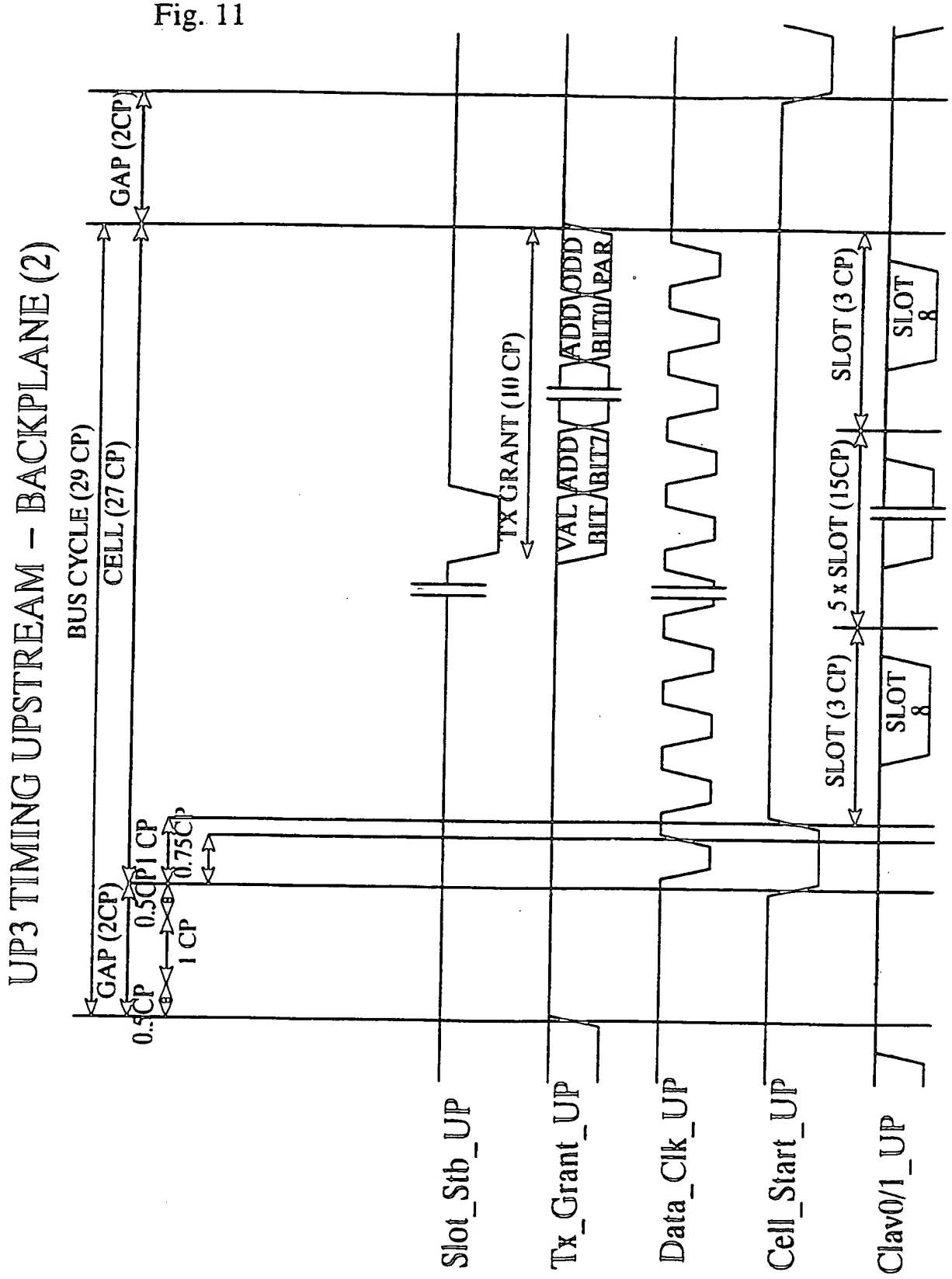

UP3 TIMING UPSTREAM – BACKPLANE (1)
BUS CYCLE (29 CP)
CELL (27 CP)
GAP (2CP)
GAP (2CP)
0.5CP
0.5CP
1 CP
1 CP
0.75CP
TX GRANT (10 CK PERIODS)
VAL BIT
ADD BIT7
ADD BIT0
ODD PAR
W1
W2
W3
W4
W23
W24
W25
W26
W27
Slot_Stb_UP
Tx_Grant_UP
Data_Clk_UP 1
Data_Clk_UP 7
Data_Clk_UP 8
Cell_Start_UP
Data_UP(15:0)
CRC6_UP(5:0)

Fig. 11



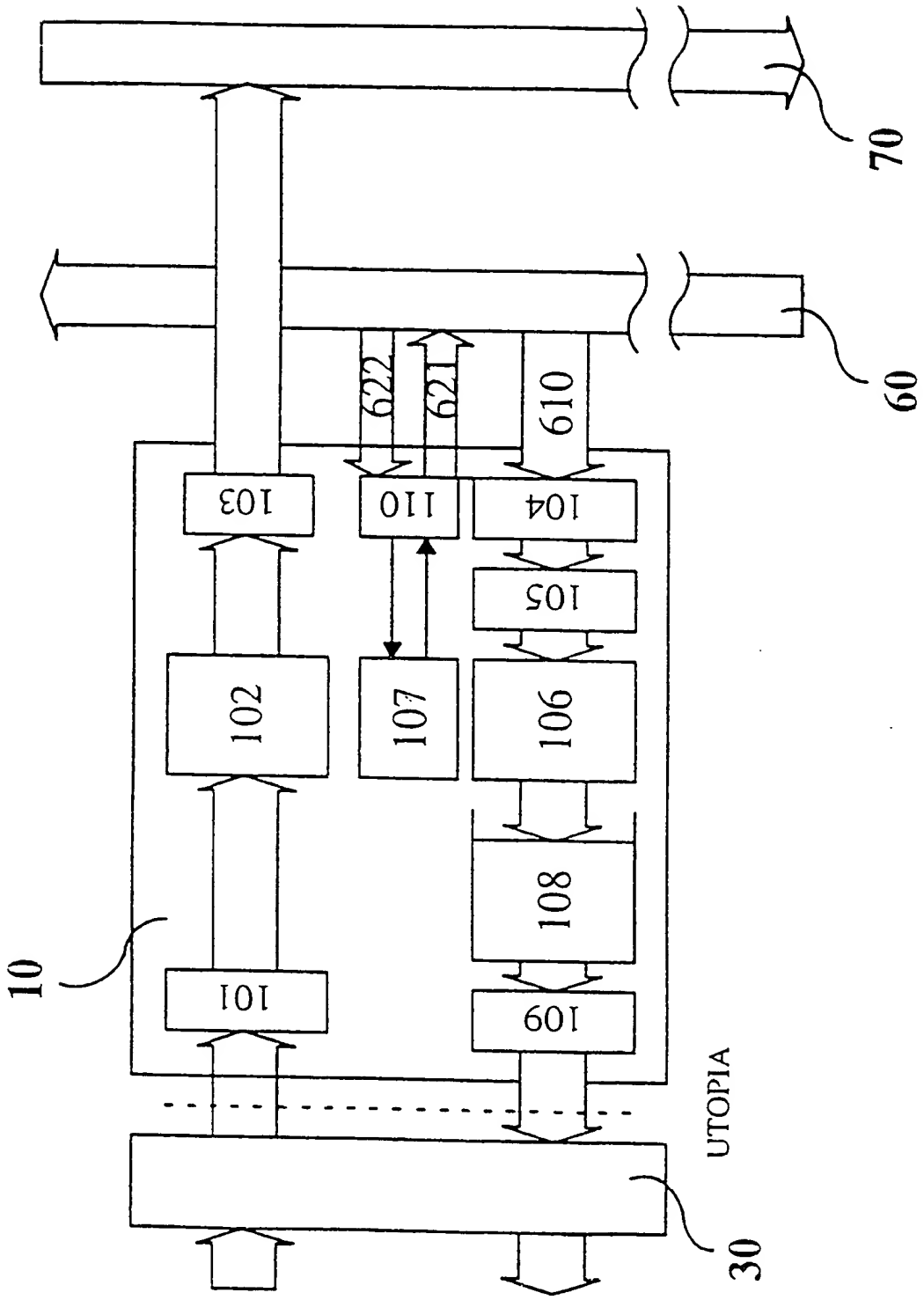

70
60
622
621
610
103
110
104
105
102
107
106
108
10
101
109
UTOPIA
30

Fig. 12

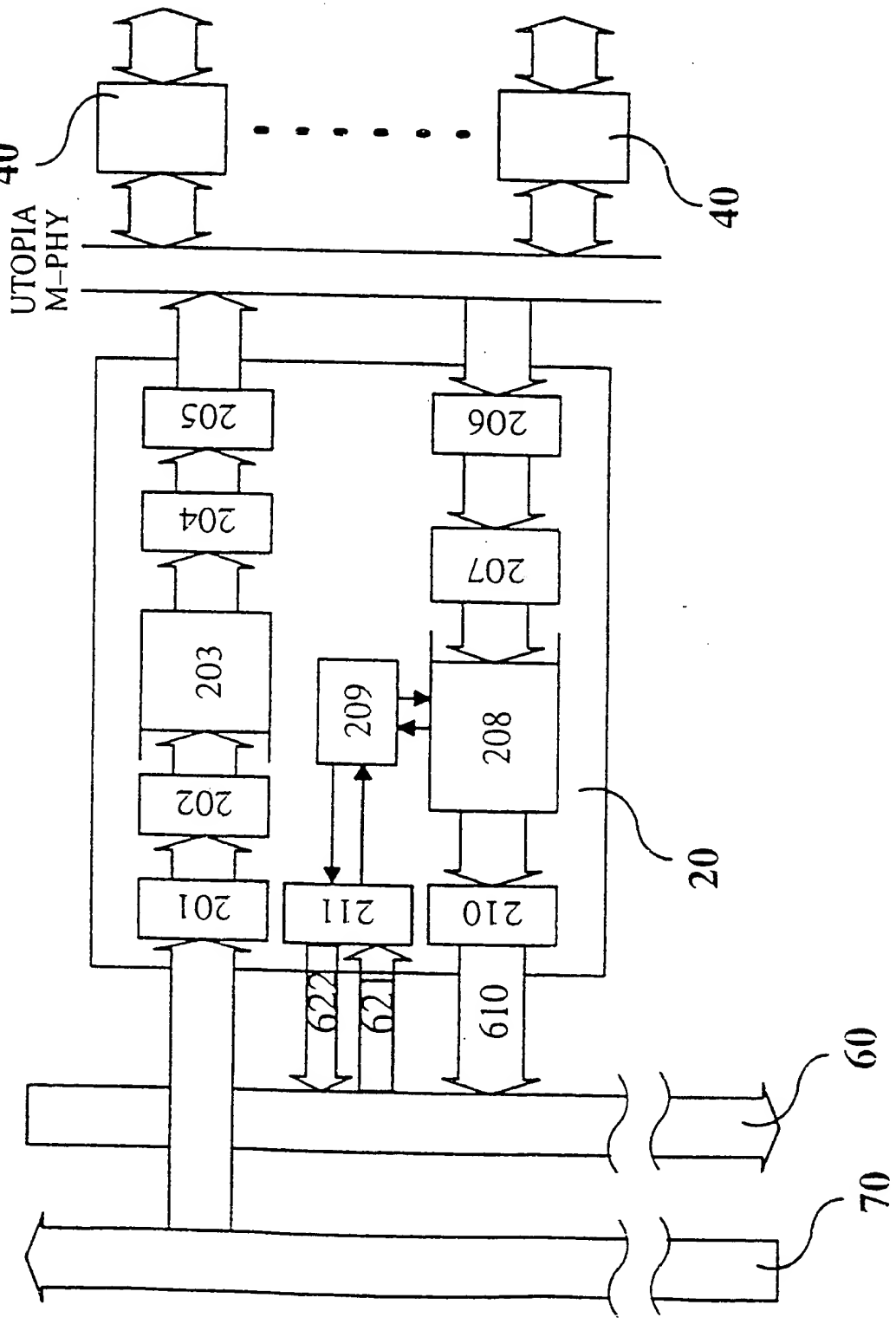


Fig. 13

INTERNATIONAL SEARCH REPORT

Inter nal Application No
PCT/EP 98/00856

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04L12/56

According to International Patent Classification(IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 95 08887 A (TRANSWITCH CORP) 30 March 1995 cited in the application see abstract; claim 1	1
A	SMITH J C: "AN INNOVATIVE ATM SWITCH USING EXISTING FOUR-PORTTM TECHNOLOGY" SOUTHCON /94. CONFERENCE RECORD, ORLANDO, MAR. 29 - 31, 1994, 29 March 1994, INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, pages 607-614, XP000544446 see page 607, left-hand column, paragraph 3 - page 609, right-hand column, paragraph 2	1

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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Date of the actual completion of theinternational search	Date of mailing of the international search report
2 July 1998	15/07/1998

Name and mailing address of the ISA	Authorized officer
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1

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INTERNATIONAL SEARCH REPORT

Information on patent family members

Interr nal Application No
PCT/EP 98/00856

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 9508887 A	30-03-1995	AU 7838894 A	10-04-1995
		CA 2170602 A	30-03-1995
		CN 1134207 A	23-10-1996
		EP 0724796 A	07-08-1996
		JP 9504919 T	13-05-1997